ADFP Cloud 2.0

軟體使用 EDA Tool 指引

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1. ADFP Cloud 2.0 EDA Tool 使用方法

1.1 Full-Custom EDA 軟體安裝版本列表

CAD tool for Full-custom Design					
Vendor	**Tool**	**Version**	**Source file**	**Command**	**Note**
Synopsys	HSPICE	*2020.03-sp2-2	/RAID2/cad/synopsys/hspice	hspice	Circuit Simulation
Synopsys	FineSim	2022.06	/RAID2/cad/synopsys/finesim	finesim	Fast Circuit Simulation
Synopsys	CustomSim	2022.06	/RAID2/cad/synopsys/xa	xa	Mixed Signal Simulation
Synopsys	PrimeSim	2022.06	/RAID2/cad/synopsys/primesim	primesim	Fast GPU-accelerated Simulator
Cadence	SPECTRE	*19.10.322	/RAID2/cad/cadence/SPECTRE	virtuoso	Mixed-signal simulation
Synopsys	CustomExplorer	2022.06	/RAID2/cad/synopsys/customexplorer	wv	Waveform
Cadence	IC6	06.18.250	/RAID2/cad/cadence/IC	virtuoso	Virtuoso Analog Design Environment
Cadence	ICADVM	*18.10.130	/RAID2/cad/cadence/ICADVM	virtuoso	Virtuoso Analog Design Environment
Synopsys	CustomCompiler	*2020.12-sp1-2	/RAID2/cad/synopsys/customcompiler	cc	Layout Tool
Synopsys	Laker_OA	2021.06	/RAID2/cad/synopsys/laker_oa	laker	Layout Tool
Cadence	LIBERATE	21.72.187	/RAID2/cad/cadence/LIBERATE	liberate	Library Characterization
Synopsys	SiliconSmart	2022.12	/RAID2/cad/synopsys/siliconsmart	siliconsmart	Library Characterization
Synopsys	Library Compiler	2022.03	/RAID2/cad/synopsys/lc	lc_shell	Library Compiler
Siemens	Calibre	*2019.2_26.18	/RAID2/cad/mentor/calibre	calibre	DRC/LVS/PEX
Synopsys	IC_Validator	*2021.06-sp2	/RAID2/cad/synopsys/icvalidator	icv	DRC/LVS
Cadence	QUANTUS	*21.11.000	/RAID2/cad/cadence/QUANTUS		RC Extractioin
Synopsys	Star-RCXT	*2019.12-sp5-3	/RAID2/cad/synopsys/star-rcxt		RC Extractioin

1.2 Full-Custom EDA 軟體使用指令參考

(1) Hspice

單核心: hspice demo.sp -o out.log

多核心: hspice demo.sp -hpp -mt 4 -o out.log

（2） Virtuoso / ICADVM

source /usr/cad/cadence/CIC/ICADVM.cshrc （only for FinFET）

virtuoso &

Remember to setup .cdsenv / .cdsinit / cds.lib

（sample file include in /RAID2/cshrc/virtuoso/）

1.3 Cell-Based EDA 軟體安裝版本列表

CAD tool for Cell-based Design					
Vendor	**Tool**	**Version**	**Source file**	**Command**	**Note**
Synopsys	Verdi	2019.06	/RAID2/cad/synopsys/verdi	nWave	Waveform
Synopsys	VCS	2022.06	/RAID2/cad/synopsys/vcs	vcs	HDL Simulation tool
Cadence	INCISIVE	15.20.084	/RAID2/cad/cadence/INCISIV	irun	HDL Simulation tool
Cadence	XCELIUM	22.03.003	/RAID2/cad/cadence/XCELIUM	xrun	HDL Simulation tool
Synopsys	Design_Compiler	2022.03	/RAID2/cad/synopsys/synthesis	dcnxt_shell, dv	Logic Synthesis tool
Synopsys	Design_Compiler	*2019.03-sp1-1	/RAID2/cad/synopsys/synthesis	dc_shell, dv	Logic Synthesis tool
Cadence	GENUS	20.10.000	/RAID2/cad/cadence/GENUS	genus	Logic Synthesis tool
Cadence	INNOVUS	*20.15.000	/RAID2/cad/cadence/INNOVUS	innovus	Auto Placement and Routing
Synopsys	IC Compiler 2	*2021.06-sp5	/RAID2/cad/synopsys/icc2	icc2	IC Compiler 2 Auto Placement and Routing
Synopsys	IC Compiler	2022.03	/RAID2/cad/synopsys/icc	icc	IC Compiler Auto Placement and Routing
Cadence	JASPER	2021.03	/RAID2/cad/cadence/JASPER	jg	Formal Verification
Synopsys	VC_Formal	*2020.03-1	/RAID2/cad/synopsys/vc_formal	vcf	Formal Verification
Synopsys	PrimeTime	*2019.03-sp5-1	/RAID2/cad/synopsys/primetime	pt_shell	Power analysis / STA
Cadence	SSV-Tempus	*21.12.000	/RAID2/cad/cadence/SSV		Tempus Timing Signoff Solution
Cadence	PEGASUS	*21.20.000	/RAID2/cad/cadence/PEGASUS		DRC Tool

1.4 Cell-Based EDA 軟體使用指令參考

(2) irun/xrun

單核心: irun TESTBED.v -define RTL -define FUNC -debug -f file_list.f -incdir /usr/cad/synopsys/synthesis/cur/dw/sim_ver/ -notimingchecks -loadpli1 debpli:novas_pli_boot

多核心: xrun -mcl 4 TESTBED.v -define RTL -define FUNC -debug -f file_list.f -incdir /usr/cad/synopsys/synthesis/cur/dw/sim_ver/ -notimingchecks -loadpli1 debpli:novas_pli_boot

(3) Design Compiler / Prime Time

dcnxt_shell -f syn.tcl | tee syn.log

pt_shell -f ptpx.tcl | tee CORE_power.log

多核心 ---> set_host_options -max_cores 4 in your .tcl file

(4) Innovus

innovus &

setMultiCpuUsage -localCpu 4

(5)VCS

多核心: vcs +v2k -sverilog -R -full64 +define+FUNC +define+RTL TESTBED.v -debug_access+all -l vcs.log -P /usr/cad/synopsys/verdi/2019.06/share/PLI/VCS/linux64/novas.tab /usr/cad/synopsys/verdi/2019.06/share/PLI/VCS/linux64/pli.a -y /usr/cad/synopsys/synthesis/cur/dw/sim_ver/ +incdir+/usr/cad/synopsys/synthesis/cur/dw/sim_ver/ +libext+.v -f file_list.f +notimingchecks -j4

1.5 自定義預設環境 .tcshrc

使用者可以自己定義要 source 那些軟體，並且指定所需要的 license server。

vim ~/.tcshrc

```
setenv CDS_AUTO_64BIT ALL
source /RAID2/cad/synopsis/CIC/hspice.cshrc
source /RAID2/cad/cadence/CIC/ic.cshrc
setenv MGLS_LICENSE_FILE 1717@lshc
setenv LM_LICENSE_FILE 1717@lshc:5280@lshc:26585@lshc
...
alias     btop        'btop --utf-force -t'
```

1.6 合成與模擬軟體常用檔案路徑

Design Ware 模擬檔案路徑:

/usr/cad/synopsys/synthesis/cur/dw/sim_ver/

標準元件庫模擬檔案路徑:

/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/VERILOG/N16ADFP_StdCell.v

標準元件 IO 庫模擬檔案路徑:

/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/VERILOG/N16ADFP_StdIO.v

SRAM IP 庫模擬檔案路徑:

/ADFP/Executable_Package/Collaterals/IP/sram/N16ADFP_SRAM/VERILOG/N16ADFP_SRAM_100a.v

標準元件庫合成 db/lib 檔案路徑:

/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM

標準元件 IO 庫合成 db/lib 檔案路徑:

/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM

SRAM IP 庫合成 db/lib 檔案路徑:

/ADFP/Executable_Package/Collaterals/IP/sram/N16ADFP_SRAM/NLDM